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EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/735,899	Applicant(s) JOURDAN ET AL.	
	Examiner Barry J. O'Brien	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2000 and 07 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration as received on 5/7/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The disclosure is objected to because of the following informalities:

   a. On pages 3-5, reference number 230 of Fig.2 is referred to as "instruction cache", "cache memory", and "internal cache", while Figure 2 only refers to it as "instruction cache." Please update the specification to use consistent terminology.

5. Appropriate correction is required.

Claim Objections

6. Claims 2-4 and 6-9 are objected to because of the following informalities:

   a. Regarding claims 2, 4, 7 and 9, please insert the word "were" before the phrase "assembled into the instruction segment" in order to be grammatically correct.

b. Regarding claims 3 and 8, please insert the word "was" before the phrase "assembled into the instruction segment" in order to be grammatically correct.

c. Regarding claim 6, please make the word "instruction" in the phrase "instruction in the instruction segment" plural, so that the phrase reads "instructions in the instruction segment", in order to be grammatically and functionally correct.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kranich et al, U.S. Patent No. 6,185,675.

10. Regarding claim 1, Kranich has taught an instruction segment storing method, comprising:

a. Building an instruction segment (see Col.3 lines 60-62),

b. Determining whether the instruction segment satisfies a filtering condition,

c. If the instruction segment satisfies the filtering condition, storing the instruction segment in a segment cache (see Col.4 line 1).

11. While not shown explicitly, it is inherent that Kranich teaches the satisfaction of a filtering condition. Because the claim language does not define what a "filtering condition" consists of, and because Kranich has taught the storing of the instruction segment in a segment cache, it is inherent that a filtering condition has been met, otherwise the instruction segment would not have been stored (see Col.3 lines 60-67 and Col.4 lines 1-9). Furthermore, the "filtering condition" can be considered to be whether the instruction segment was a basic block that ended with a branch instruction, in which case the filtering condition would inherently always be satisfied when the basic blocks were stored in the segment cache.

12. Regarding claims 2 and 7, taking claim 2 as exemplary, Kranich has taught the method of claim 1, wherein the filtering condition may be met only if all instructions in the instruction segment were assembled into the instruction segment from an instruction cache of a front-end processing system in a processor, although it was not taught explicitly. Kranich has taught that all instructions that were used to create instruction segments came from the instruction cache (see Col.7 line 17 and Col.8 lines 4-10). As described above in paragraph 7, the filtering condition can be considered to be whether the instruction segment was a basic block. Therefore, Kranich has inherently taught that the filtering condition has been met and that all instructions in the instruction segment came from the instruction cache.

13. Claim 7 is nearly identical to claim 2, differing only in its parent claim, which is rejected accordingly below, and in minor informalities in its claim language. Therefore, claim 7 is rejected for the same reasons as claim 2.

14. Regarding claims 3 and 8, taking claim 3 as exemplary, Kranich has taught the method of claim 1, wherein the filtering condition may be met only if at least one instruction in the

instruction segment was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor, although it was not taught explicitly. Kranich has taught that all instructions used to create instruction segments came from the instruction cache (see Col.7 line 17 and Col.8 lines 4-10). Also, as described above in paragraph 7, the filtering condition can be considered to be whether the instruction segment was a basic block. Therefore, because Kranich has taught all the instructions being from the instruction cache, which inherently contains at least one instruction, Kranich has taught the filtering condition having been met and that at least one of the instructions in the instruction segment has come from the instruction cache.

15. Claim 8 is nearly identical to claim 3, differing only in its parent claim, which is rejected accordingly below, and in minor informalities in its claim language. Therefore, claim 8 is rejected for the same reasons as claim 3.

16. Regarding claims 4 and 9, taking claim 4 as exemplary, Kranich has taught the method of claim 1, wherein the filtering condition may be met only if a predetermined number of instructions in the instruction segment were assembled into the instruction segment from an instruction cache of a front-end processing system in a processor, although not taught explicitly. Kranich has taught that all instructions used to create instruction segments come from the instruction cache (see Col.7 line 17 and Col.8 lines 4-10), as well as basic blocks being padded if there are less than a predetermined number of instructions in the block in order to create equal size basic blocks (see Col.3 lines 60-65). Also, as described above in paragraph 7, the filtering condition can be considered to be whether the instruction segment was a basic block. Therefore, because Kranich has taught all the instructions being from an instruction cache, and the basic

blocks having at least a predetermined number of instructions within them, then Kranich has inherently taught the filtering condition having been met and a predetermined number of instructions in the instruction segment having come from the instruction cache.

17. Claim 9 is nearly identical to claim 4, differing only in its parent claim, which is rejected accordingly below, and in minor informalities in its claim language. Therefore, claim 9 is rejected for the same reasons as claim 4.

18. Regarding claims 5 and 10, taking claim 5 as exemplary, Kranich has taught the method of claim 1, wherein the filtering condition may be met only if an instruction of the segment by which the segment is to be indexed was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor, although not explicitly. Kranich has taught that all instructions used to create instruction segments come from the instruction cache (see Col.7 line 17 and Col.8 lines 4-10). Also, as described above in paragraph 7, the filtering condition can be considered to be whether the instruction segment was a basic block. Therefore, because Kranich has taught all the instructions in the segment being from an instruction cache, and because basic blocks inherently have an instruction used to index them into the cache (see Col.3 lines 60-67 and Col.4 lines 1-9), then Kranich has inherently taught the filtering condition having been met and an instruction of the segment which indexes it having come from the instruction cache.

19. Claim 10 is nearly identical to claim 5, differing only in its parent claim, which is rejected accordingly below, and in minor informalities in its claim language. Therefore, claim 10 is rejected for the same reasons as claim 5.

20. Regarding claim 6, Kranich has taught an instruction segment storing method, comprising:

a. Building an instruction segment (see Col.3 lines 60-62),

b. Determining, from location flags associated with instructions in the instruction segment, whether the instruction segment satisfies a filtering condition,

c. If so, storing the instruction segment in a segment cache (see Col.4 line 1).

21. While not shown explicitly, it is inherent that Kranich teaches the satisfaction of a filtering condition from location flags associated with instructions in the instruction segment. Because the claim language does not define what a "filtering condition" or "location flags" consist of, and because Kranich has taught the storing of the instruction segment in a segment cache, it is inherent that a filtering condition has been met using the location flags, otherwise the instruction segment would not have been stored (see Col.3 lines 60-67 and Col.4 lines 1-9). Furthermore, the "filtering condition" can be considered to be whether the instruction segment was a basic block that ended with a branch instruction, in which case the filtering condition would inherently be met when the basic blocks were stored in the segment cache. Also, the basic block cache stores an address tag with each instruction in the basic block (see Col.8 lines 7-10) that can be considered a "location flag" because it describes the location within the segment and cache of the instruction, in which case the "location flags" are associated with the instructions that meet the "filtering condition".

22. Regarding claims 11 and 18, taking claim 11 as exemplary, Kranich has taught a front-end system for a processing agent, comprising:

a. An instruction cache system (16 of Fig.2),

b. An instruction segment system comprising:

i. A segment cache (44 of Fig.2),

ii. A segment builder (20 of Fig.2) provided in communication with the instruction cache system, to store a new instruction segment in the segment cache when a filtering condition is met (see Col.8 lines 4-10).

23. While not taught explicitly, it is inherent that Kranich teaches the satisfaction of a filtering condition. Because the claim language does not define what a "filtering condition" consists of, and because Kranich has taught the storing of the instruction segment in a segment cache, it is inherent that a filtering condition has been met, otherwise the instruction segment would not have been stored (see Col.3 lines 60-67 and Col.4 lines 1-9). Furthermore, the "filtering condition" can be considered to be whether the instruction segment was a basic block that ended with a branch instruction, in which case the filtering condition would inherently be met when the basic blocks were stored in the segment cache.

24. Claim 18 is nearly identical to claim 11. It differs only in its addition of a cache hierarchy, which Kranich has taught (see Col.6 lines 21-24), further in communication with the instruction cache system (see Fig.2), as well as in minor informalities in its claim language. Therefore, claim 18 is rejected for the same reasons as claim 11.

25. Regarding claims 12 and 19, taking claim 12 as exemplary, Kranich has taught the front-end system of claim 11, further comprising a history map (42 of Fig.2) provided in communication with the segment builder to identify when the filtering condition is met. While not taught explicitly, it is inherent that the basic block sequence buffer (BBSB) (42 of Fig.2) identifies when the filtering condition has been met. As described above in paragraph 19, the

filtering condition can be considered to be whether the instruction segment was a basic block ending with a branch instruction. Kranich has taught the BBSB storing information about the instructions, including prediction about the branch instruction that ends the basic block (see Col.8 lines 23-31). Therefore, because Kranich has inherently taught the BBSB identifying when the filtering condition was met, because if the condition was not met, no information about the branch instruction within the basic block would have been stored in the BBSB.

26. Claim 19 is nearly identical to claim 12. It differs only in its parent claim, and in minor informalities in its claim language. Therefore, claim 19 is rejected for the same reasons as claim 12.

27. Regarding claim 13, Kranich has taught the front-end system of claim 12, wherein the history map is a direct mapped cache (see Col.8 lines 10-13). While not taught explicitly, Kranich has taught the BBSB (42 of Fig.2) having the same structure as the Basic Block Cache (BBC), which in one embodiment is a set-associative cache (see Col.8 lines 20-23). Also, it is well known in the art that a direct mapped cache is simply a one-way set associative cache (see Patterson and Hennessy, *Computer Organization and Design*, 2nd Ed., 1998, p.570). Therefore, because Kranich has taught a set-associative BBSB, it being a direct mapped cache has also been taught.

28. Regarding claim 14, Kranich has taught the front-end system of claim 12, wherein the history map is a set associative cache (see Col.8 lines 10-13). While not taught explicitly, Kranich has taught the BBSB (42 of Fig.2) having the same structure as the Basic Block Cache (BBC), which in one embodiment is a set-associative cache (see Col.8 lines 20-23). Therefore, Kranich has taught a set-associative BBSB.

29. Regarding claim 15, Kranich has taught the front-end system of claim 14, wherein the history map (42 of Fig.2) comprises a plurality of cache entries having a width corresponding to a width of a tag address of an instruction pointer in the system (see Col.8 lines 9-11). While not taught explicitly, Kranich has taught the BBSB (42 of Fig.2) having the same structure as the Basic Block Cache (BBC), which in one embodiment is a set-associative cache (see Col.8 lines 20-23). Also, it is well known in the art that a direct mapped cache is simply a one-way set associative cache (see Patterson and Hennessy, *Computer Organization and Design*, 2nd Ed., 1998, p.570). Therefore, Kranich has taught the BBSB having an entire fetch address as a tag and entry into itself.

30. Regarding claim 16, Kranich has taught the front-end system of claim 14, wherein the history map (42 of Fig.2) comprises a plurality of cache entries having a width corresponding to a width of a portion of a tag address of an instruction pointer in the system (see Col.8 lines 11-19).

31. Regarding claims 17 and 20, taking claim 20 as exemplary, Kranich has taught the processing agent of claim 18, wherein:

a. The instruction cache system outputs instructions (see Col.7 lines 16-17 and 56-57) and location flags to the segment builder (20 of Fig.2), the location flags distinguishing instructions retrieved from the instruction cache system from instructions retrieved from the cache hierarchy,

b. The segment builder determining whether the filtering condition is met based on location flags associated with instructions of the new instruction segment.

32. While not shown explicitly, it is inherent that Kranich teaches the location flags distinguishing instructions as well as the satisfaction of a filtering condition from location flags associated with instructions in the instruction segment. Because the claim language does not define what a "filtering condition" or "location flags" consist of, and because Kranich has taught the storing of the instruction segment in a segment cache, it is inherent that a filtering condition has been met using the location flags, otherwise the segment builder would not have stored the instruction segment (see Col.3 lines 60-67 and Col.4 lines 1-9). Furthermore, Kranich has taught that the basic block cache stores an address tag with each instruction in the basic block (see Col.8 lines 7-10) that can be considered a "location flag" because all instructions that had this tag came from the instruction cache. Also, the "filtering condition" can be considered to be whether the instruction segment was a basic block that ended with a branch instruction, in which case the filtering condition would inherently be met when the basic blocks were stored in the segment cache. Therefore, the segment builder (20 of Fig.2) determined if the filtering condition was met with regards to the location flags and subsequently stored the instruction segment.

33. Regarding claim 21, Kranich has taught a computer system comprising the processing agent of claim 18, wherein the cache hierarchy includes an internal cache and a system memory (see Col.6 lines 21-24).

34. Regarding claim 22, Kranich has taught a computer system comprising the processing agent of claim 18, wherein the cache hierarchy includes an internal cache (see Col.6 lines 21-24) and an external cache (see Col.2 lines 26-29).

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

36. Miller, U.S. Patent No. 6,339,822 has taught a basic block cache with padded instructions within the blocks containing information about the instructions and their segments.

37. Peleg et al, U.S. Patent No. 5,381,533 has taught an instruction trace cache with traces that can cross address line boundaries.

38. Rotenberg et al, *Trace Processors*, has taught the use of trace caches in microprocessors in order to speed up instruction execution.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
10/27/2003

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